

CLAIMS

What is claimed is:

1. A synchronous memory comprising:
 - a clock input signal;
 - 5 an adjustable delay line for generating a data output driving clock signal from the clock input signal; and
 - a data output buffer enabled by the driving clock signal for outputting data to an output terminal, the data being output to the output terminal at the same time as or a minimum time following an edge of the clock input signal.
- 10 2. Synchronous memory as claimed in claim 1 wherein the adjustable delay line is in a delay locked loop.
3. Synchronous memory as claimed in claim 2 wherein the delay locked loop further comprises a delay model circuit which uses similar elements as the real circuit path.
- 15 4. Synchronous memory as claimed in claim 2 wherein the adjustable delay line is a tapped delay line.
5. Synchronous memory as claimed in claim 4 wherein taps provide plural outputs of the delay line.
6. Synchronous memory as claimed in claim 1 wherein the adjustable delay line is
20 adapted to be disabled as a clock source to the data output buffer.

7. Synchronous memory as claimed in claim 1 wherein the adjustable delay line is used only to enable the data output buffer.
8. A synchronous dynamic random access memory comprising:
 - a clock input signal;
 - 5 a delay locked loop comprising an adjustable delay line for generating a data output driving clock signal from the clock input signal; and
 - a data output buffer enabled by the driving clock signal for outputting data to an output terminal, the data being output to the output terminal at the same time as or a minimum time following an edge of the clock input signal.
- 10 9. A method of enabling synchronous memory data output comprising:
 - delaying a clock input signal in an adjustable delay line to generate a data output driving clock signal; and
 - enabling output data with the driving clock signal, the data being output to an output terminal at the same time as or a minimum time following an edge
 - 15 of the clock input signal.
10. A method of enabling synchronous memory data output as claimed in claim 9 wherein the adjustable delay line is in a delay locked loop.
11. A method of enabling synchronous memory data output as claimed in claim 10 wherein the delay locked loop further comprises a delay model circuit which
- 20 uses similar elements as the real circuit path.
12. A method of enabling synchronous memory data output as claimed in claim 10 wherein the adjustable delay line is a tapped delay line.

13. A method of enabling synchronous memory data output as claimed in claim 12 wherein taps provide plural outputs of the delay line.
14. A method of enabling synchronous memory data output as claimed in claim 9 further comprising disabling the adjustable delay line as a clock source for enabling output data.
15. A method of enabling synchronous memory data output as claimed in claim 9 wherein the adjustable delay line is used only to enable output data.
16. A method of enabling synchronous random access memory data output comprising:
 - 10 delaying a clock input signal in an adjustable delay line of a delay locked loop to generate a data output driving clock signal; and
 enabling output data with the driving clock signal, the data being output to an output terminal at the same time as or a minimum time following an edge of the clock input signal.
- 15 17. A synchronous dynamic random access memory comprising:
 - means for delaying a clock input signal in an adjustable delay line of a delay locked loop to generate a data output driving clock signal; and
 means for enabling output data with the driving clock signal, the data being output to an output terminal at the same time as or a minimum time
20 following an edge of the clock input signal.